Code: 19CS3301, 19IT3301

II B.Tech - I Semester – Regular Examinations – MARCH 2021

FUNDAMENTALS OF DIGITAL LOGIC DESIGN

(Common to CSE, IT)

Duration: 3 hours Max. Marks: 70

Note: 1. This question paper contains two Parts A and B.
2. Part-A contains 5 short answer questions. Each Question carries 2 Marks.
3. Part-B contains 5 essay questions with an internal choice from each unit. Each question carries 12 marks.
4. All parts of Question paper must be answered in one place

PART – A

1. a) Perform the following division in binary: 111011 ÷101
b) What are universal gates? Why they are called universal gates?
c) List the steps involved in design procedure of combinational circuits.
d) Differentiate between combinational and sequential circuits.
e) Write any two differences between Ring counter & Johnson counter.

PART – B

UNIT – I

2. a) Represent the decimal number 5137 in
(i) BCD (ii) Excess-3 code
(iii) 2421 code (iv) 6311 code. 8 M
b) Find the 9's and the 10's complement of the following decimal number: 52,784,630 4 M

OR

3. a) Add and multiply the following numbers without converting them to decimal
   i. Binary numbers 1011 and 101.
   ii. Hexadecimal numbers 2E and 34. 8 M

   b) Convert the decimal number 431 to binary in two ways:
   i. Convert directly to binary;
   ii. Convert first to hexadecimal and then from hexadecimal to binary. Which method is faster? 4 M

UNIT – II

4. With the use of maps, find the simplest sum-of-products form of the function $F = fg$ and draw corresponding logic diagram where
$f = abc' + c'd + a'cd' + b'cz'$ and
$g = (a + b + c' + d')(b' + c' + d)(a' + c + d')$ 12 M

OR

5. Find the SOP and POS forms of the following Boolean function using K-map and draw the corresponding logic diagrams:
$$F(A, B, C) = \sum m(0, 2, 8, 9, 10, 15) + d(1, 3, 6, 7)$$ 12 M

UNIT-III

6. Implement 1-bit full adder with following steps:
   i. Symbolic representation
   ii. Truth table
   iii. K-map
   iv. Logic diagram 12 M

OR

7. a) Design a combinational logic that can add two 4-bit BCD numbers. 6 M

b) Write the truth table of 3-bit gray to binary code conversion. Show the realization using 4:1MUXs. 6 M

UNIT – IV

8. a) A sequential circuit consists of a full-adder circuit connected to a D flip-flop, as shown in Fig. 1. Derive the state table and state diagram of the sequential circuit.

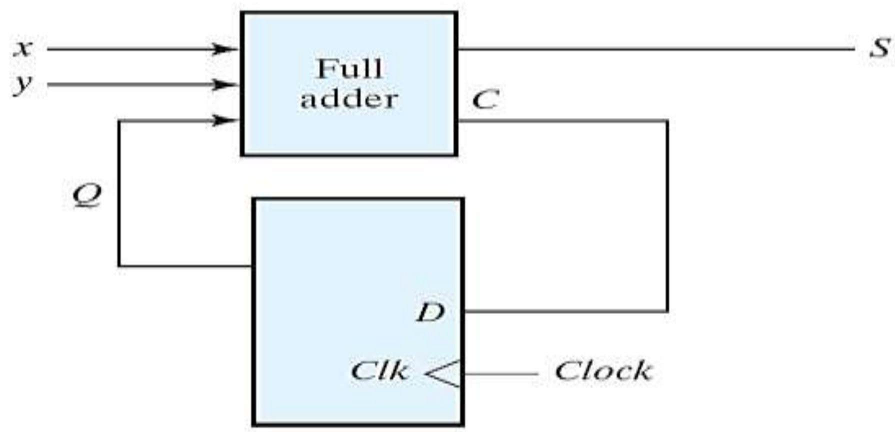

Fig. 1.

6 M

b) Show that the characteristic equation for the complement output of a JK flip-flop is

$Q'(t + 1) = J'Q' + KQ.$ 6 M

OR

9. a) Draw the logic diagram of positive edge triggered S-R flip-flop and explain its operation with the help of truth table. 6 M

b) Describe the following with truth table and block diagram:

i. JK flip-flop   ii. D flip-flop

and convert JK flip-flop to D flip-flop   6 M

UNIT – V

10. a) Design a synchronous Mod-6 counter using clocked JK flip-flops sequence given is 0-2-3-6-5-1.   6 M

b) Implement a 3-bit ripple down counter using edge triggered T flip-flops and also write the appropriate truth table.   6 M

OR

11. Design a counter with T flip-flops that goes through the following binary repeated sequence: 0, 1, 3, 7, 6, 4. Show that when binary states 010 and 101 are considered as don't care conditions, the counter may not operate properly. Find a way to correct the design.   12 M